We Claim:

1. An integrated transformer configuration, comprising:

a first coil formed from an electrically conductive material having a spiral course with an essentially rectangular cross section; and

a second coil having a spiral course;

said first coil and said second coil being electrically insulated from one another;

said rectangular cross section of said first coil a height and a width; and

a ratio between said height and said width of said rectangular cross section of said first coil being greater than 1.

2. The semiconductor configuration according to claim 1, wherein said ratio between said height and said width of said rectangular cross section of said first coil is greater than 3.

3. The semiconductor configuration according to claim 1, further comprising:

a first semiconductor body formed with a first trench having a spiral course and extending vertically into said semiconductor body;

said first coil being formed in said first trench.

4. The semiconductor configuration according to claim 3, further comprising:

a second semiconductor body;

said second coil formed in or on said second semiconductor body;

said first semiconductor body and said second semiconductor body configured one above another; and

said first semiconductor body and said second semiconductor body being insulated from one another.

5. The semiconductor configuration according to claim 3, further comprising:

a second semiconductor body; and

an insulation layer formed between said first semiconductor body and said second semiconductor body;

said first semiconductor body and said second semiconductor body configured one above another;

said first semiconductor body and said second semiconductor body being insulated from one another by said insulation layer; and

said second coil formed in said insulation layer.

6. The semiconductor configuration according to claim 3, further comprising:

an insulation layer formed above said first semiconductor body;

said second coil formed in said insulation layer.

7. The semiconductor configuration according to claim 6, further comprising:

a metalization plane;

said insulation layer being part of said metalization plane.

8. The semiconductor configuration according to claim 3, wherein:

said second coil is formed above or below said first coil; and

said second coil is formed in said first trench.

9. The semiconductor configuration according to claim 3, wherein said first semiconductor body includes a heavily doped semiconductor material forming said second coil.

10. The semiconductor configuration according to claim 9, wherein said heavily doped semiconductor material forming said second coil is formed below said first trench with said first coil.

11. The semiconductor configuration according to claim 9, wherein said heavily doped semiconductor material forming said second coil is formed adjacent said first trench with said first coil.

12. The semiconductor configuration according to claim 1, further comprising:

a semiconductor body; and

an insulation layer formed above said semiconductor body;

said first coil formed in said insulation layer.

13. The semiconductor configuration according to claim 12, further comprising:

a metalization plane;

said insulation layer being part of said metalization plane.

14. The semiconductor configuration according to claim 12, wherein:

said second coil is formed above said semiconductor body; and

said second coil is formed in said insulation layer and is insulated from said semiconductor body.

15. The semiconductor configuration according to claim 14, wherein said second coil is formed between said first coil and said semiconductor body.

16. The semiconductor configuration according to claim 12, wherein said second coil is formed in said semiconductor body.

17. The semiconductor configuration according to claim 16, wherein said second coil is formed from a heavily doped semiconductor material.

18. The semiconductor configuration according to claim 12, wherein:

said first coil is formed from a plurality of component coils configured one above another in said insulation layer; and

said plurality of component coils are electrically connected to one another.

19. The semiconductor configuration according to claim 1, wherein said semiconductor body is part of an SOI substrate.

20. The semiconductor configuration according to claim 1, further comprising:

a transmitting device connected to one coil selected from a group consisting of said first coil and said second coil; and

a receiver device connected to another coil selected from a group consisting of said first coil and said second coil.

21. The semiconductor configuration according to claim 20,

a first semiconductor body formed with a first trench having a spiral course and extending vertically into said semiconductor body, said first coil being formed in said first trench;

a second semiconductor body, said second coil formed in or on said second semiconductor body, said first semiconductor body and said second semiconductor body configured one above another, said first semiconductor body and said second semiconductor body being insulated from one another;

a transmitting device integrated in one semiconductor body selected from a group consisting of said first semiconductor body and said second semiconductor body; and

a receiver device integrated in another semiconductor body selected from a group consisting of said first semiconductor body and said second semiconductor body.

22. The semiconductor device according to claim 1, further comprising:

a first semiconductor body formed with a first trench having a spiral course and extending vertically into said semiconductor body, said first coil being formed in said first trench, said

second coil formed above or below said first coil, said second coil formed in said first trench; and

a transmitter device and a receiver device integrated in said first semiconductor body.

23. The semiconductor device according to claim 1, further comprising:

a plurality of semiconductor bodies including a first semiconductor body formed with a first trench having a spiral course and extending vertically into said semiconductor body, said first coil being formed in said first trench, said second coil formed above or below said first coil, said second coil formed in said first trench; and

a transmitting device and a receiver device integrated in different ones of said plurality of semiconductor bodies; and

one of said transmitting device and said receiver device being integrated in said first semiconductor body.